UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,782	07/28/2003	Seiji Kaneko	H-1195	5210

24956 7590 04/06/2006

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,782	KANEKO ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14,18-20 and 24* is/are rejected.

7)☒ Claim(s) *15-17 and 21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 11/628,782 has a total of 23 claims pending in the application; claims 1, 7, 9-10,12, 14, 18-20, and 24 have been amended; claim 5 has been canceled; no new claim has been added.

INFORMATION CONCERNING CLAIMS:

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1-4, 6-14, 18-20, and 24 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-8 of copending Application No. 11/331,083. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

2. Claims 1 of instant application (Application No. 10/628,782) are compared to claim 1 of copending application (Application No. 11/331,083) in the following table:

Application No. 10/628,782	*Application No. 11/331,083*
Claim 1:	**Claim 1:**
A disk array device comprising:	A disk array device comprising:
a plurality of input/output channels that receive data input/output requests from at least one external device;	a plurality of input/output channels that receive data input/output requests from at least one external device;
a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;	a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;
a disk drive device;	a disk drive device;
a disk control module that performs data input/output to and from the disk drive device;	a disk control module that performs data input/output to and from the disk drive device;
at least one communication module that communicatively connects the input/output channels with the disk control module; and	at least one communication module that communicatively connects the input/output channels with the disk control module; and

a control module that controls, upon receiving a data input/output request from the at Least one external device, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second.	a control module that controls, upon receiving a data input/output request from the at Least one external device, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second. wherein when said data input/output request is a write request a determination is made whether data contained in the cache memory connected to the input/output channel which receives said write request is to be updated and whether

	the data contained in the cache memories connected to the other input/output channels are to be made invalid.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: Disk Array Device, Method for Controlling the Disk Array Device and Storage System.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

Claims 1-2, 6-7, 10-12, 18-19, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,675,264 B2 to Chen et al. (hereinafter Chen).

3. *In regard to claim 1 Chen teaches:*

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 (e.g., an external device) may issue I/o request to the storage nodes 106.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).** *For example Chen teaches that storage node 106 include logic to perform data I/O from the disk device and thus represents the function of the control module recited in the claim.*

"and at least one communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).** *For example the storage node 106 is a processing and management unit. The storage unit 106 has a host interface unit and a device end interface unit for communication between the host and disk.*

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second." **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).** *Chen teaches when a node (e.g., node i) receives a write request, it checks if data is written is currently owned by another node. If data is owned by another node (e.g. a remote node), the data owned by that node may be invalidated. After invalidation the cache in node i (the node that receives the write request) will be writtenor updated.*

4. *In regard to claim 2 Chen teaches:*

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories." **(e.g., see column 3, lines 22-24).**

5. *In regard to claims 6 and 11 Chen teaches:*

"when data stored in one of the cache memories is updated, the consistency maintaining module invalidates data stored in at least another one of the cache memories." **(e.g., see column 3, lines 66-67 to column 4, lines 1-18).**

6. *In regard to claim 7 Chen teaches:*

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 may issue I/o request to caches 112.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).** *For example Chen teaches that storage node 106 include logic to perform data I/O from the disk device and thus represents the function of the control module recited in the claim.*

"and at least one communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).** *For example the storage node 106 is a processing and management unit. The storage unit 106 has a host interface unit and a device end interface unit for communication between the host and disk.*

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).** *Chen teaches when a node (e.g., node i) receives a write request, it checks if data is written is currently owned by another node. If data is owned by another node (e.g. a remote node), the data owned by that node may be invalidated. After invalidation the cache in node i (the node that receives the write request) will be written.*

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of cache coherency requires the cache lines use identical location or region of disk or main memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided). However, Chen does not expressly teach:* "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module invalidated data stored in at least another of the cache memories."

"wherein, when data stored in one of the cache memories is updated, the consistency maintaining module invalidated data stored in at least another of the cache memories." **(e.g., column 3, lines 6-8)** *for updating the information in both mass storage systems (e.g., master and slave storage systems).*

7. In regard to claim 10 Chen teaches:

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 may issue I/o request to caches 112.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see**

column 3, lines 22-24 and lines 58-60). *For example Chen teaches that a global cache directory may be used to maintain cache coherency.*

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second." **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

8. *In regard to claim 12 Chen teaches:*

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).**

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).** *Chen teaches when a node (e.g., node i) receives a write request, it checks if data is written is currently owned by another node. If data is owned by another node (e.g. a remote node), the data owned by that node may be invalidated. After invalidation the cache in node i (the node that receives the write request) will be written.*

"wherein, when data stored in one of the cache memories is updated, the consistency maintaining module invalidated data stored in at least another of the cache memories." **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of cache coherency requires the cache lines use identical location or region of disk or main memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided). However, Chen does not expressly teach:* "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module invalidated data stored in at least another of the cache memories."

9. *In regards to claim 18, Chen teaches:*

"a method for controlling disk array device **(column 3, lines 14-31)**, the disk array device comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).**

"and at least one communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second." **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

10. In regard to claim 19 Chen teaches:

"A method for controlling a disk array device **(column 3, lines 14-31)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).**

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"receiving a data input/output request from the at least one external device;" **(e.g., see abstract).**

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, controlling execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

"wherein the consistency maintaining processing includes the step of, upon updating data stored in one of cache memories, invalidating data stored in at least another one of the cache memories," **(e.g., see column 3, lines 66-67 to column 4, lines 1-18).**

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of cache coherency requires the cache lines use identical location or region of disk or main memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided).*

11. In regard to claim 24,Chen teaches:

"A storage system **(Fig. 1)** comprising:"

"at least one external device;" **(Hosts 102 in Fig. 1).**

"a disk array device including a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"whrein the disk array device includes a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, a sequence of execution of a first operation of a response processing to respond to the at least one external device according to the data input/output request and a second operation of a consistency maintaining processing to maintain consistency of data stored in each of the cache memories such that one of said first and second operations is executed first and the other of said first and second operations is executed second." **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 8-9, 13-14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of U.S. Patent 6,275,897 B1 to Bachmat.

12. In regard to claim 8 and 13 Chen teaches all limitation recited in the base claim but does not expressly teach: "when data stored in one of the cache memories is updated, the consistency maintaining module updates data stored in at least another one of the cache memories."

Bachmat teaches: "when data stored in one of the cache memories is updated, the consistency maintaining module updates data stored in at least another one of the cache memories." **(e.g., column 3, lines 6-8)** *for updating the information in both mass storage systems (e.g., master and slave storage systems).*

Disclosures by Chen and Bachmat are analogous because both references related to storage systems.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the storage cluster taught by Chen to include cache updating disclosed by Bachmat.

The motivation for using cache updating as taught by column 2, lines 60-63 would have been to provide a new and improved caching system and methods providing remote cache utilization for mass storage subsystems.

Therefore, it would have been obvious to combine disclosures by Bachmat with Chen to obtain the invention as specified in the claim.

13. In regard to claim 9 Chen teaches:

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 may issue I/o request to caches 112.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).** *For example Chen teaches*

that storage node 106 include logic to perform data I/O from the disk device and thus represents the function of the control module recited in the claim.

"and at least one communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).** *For example the storage node 106 is a processing and management unit. The storage unit 106 has a host interface unit and a device end interface unit for communication between the host and disk.*

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).** *Chen teaches when a node (e.g., node i) receives a write request, it checks if data is written is currently owned by another node. If data is owned by another node (e.g. a remote node), the data owned by that node may be invalidated. After invalidation the cache in node i (the node that receives the write request) will be written.*

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of cache coherency requires the cache lines use identical location or region of disk or main*

memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided). However, Chen does not expressly teach: "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module update data stored in at least another of the cache memories."

Bachmat teaches: "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module updates data stored in at least another of the cache memories." **(e.g., column 3, lines 6-8)** *for updating the information in both mass storage systems (e.g., master and slave storage systems).*

14. In regard to claim 14 Chen teaches:

"A disk array device **(elements 108 in Fig.1)** comprising:"

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 may issue I/o request to caches 112.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in Fig. 1).** *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).** *For example Chen teaches that storage node 106 include logic to perform data I/O from the disk device and thus represents the function of the control module recited in the claim.*

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).** *For example the storage node 106 is a processing and management unit. The storage unit 106 has a host interface unit and a device end interface unit for communication between the host and disk.*

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"a control module that controls **(element 106 in Figs. 1-2)**, upon receiving a data input/output request from the at least one external device **(see Abstract)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of*

cache coherency requires the cache lines use identical location or region of disk or main memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided). However, Chen does not expressly teach: "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module update data stored in at least another of the cache memories."

Bachmat teaches: "wherein, when data stored in one of the cache memories is to be updated, the data stored in the one of the cache memories is updated and the data stored in at least another of the cache memories is also updated." **(e.g., column 3, lines 6-8)** *for updating the information in both mass storage systems (e.g., master and slave storage systems).*

15. In regard to claim 20 Chen teaches:

"A method for controlling disk array device **(column 3, lines 14-31)** comprising:"

"the disk array device comprising a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see abstract; column 3, lines 14-18; column 10, lines5-7; Fig. 1).** *For example each storage node 106 includes a host interface unit which represents the input/output channel recited in the claim. The hosts 102 may issue I/o request to caches 112.*

"a plurality of cache memories provided for the corresponding respective input/output channels, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 3, lines 14-16; elements 112 in**

Fig. 1). *For example each storage106 node contains both host interface unit and cache 112 and therefore the cache and the host interface unit are inherently connected.*

"a disk drive device;" **(e.g., see column 3, line 29; element 108 in Fig. 1).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 3, lines 32-39; element 108 in Fig. 1).** *For example Chen teaches that storage node 106 include logic to perform data I/O from the disk device and thus represents the function of the control module recited in the claim.*

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 3, lines 14-20).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 3, lines 22-24 and lines 58-60).**

"the controlling method comprising the steps of: receiving a data input/output request from the at least one external device;" **(see Abstract)**.

"controlling an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing," **(e.g., see column 3, lines 22-24 and lines 66-67 to column 4, lines 1-18).**

"wherein the data stored in one of the cache memories and the data stored in at least another one of the cache memories are stored in an identical storage region of the disk

drive device" **(e.g., see column 3, lines 22-24; column 4, lines12-18).** *The definition of cache coherency requires the cache lines use identical location or region of disk or main memory (see definition of cache coherency from a cache memory book by Jim Handy, the relevant section is provided). However, Chen does not expressly teach:* "wherein, when data stored in one of the cache memories is updated, the consistency maintaining module update data stored in at least another of the cache memories."

Bachmat teaches: "wherein, when data stored in one of the cache memories is to be updated, the data stored in in the one of the cache memories is updated and the data stored in at least another of the cache memories is also updated." **(e.g., column 3, lines 6-8)** *for updating the information in both mass storage systems (e.g., master and slave storage systems).*

ALLOWABLE SUBJECT MATTER

Claims 3-4, 15-16, and 21-23 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 3-4 in instant application is the combination with the inclusion of the following limitations: **wherein the consistency maintaining module performs the consistency maintaining processing depending on a content of the data input/output request.**

2. *The primary reason for allowance of claims 15-21 in instant application is the combination with the inclusion of the following limitations:* **the data input/output request includes an identifier for identifying at least one of the logical volumes that is a subject of the data input/output request, and further comprising a module that performs the control of the execution order according to the identifier included in the data input/output request.**

3. *The primary reason for allowance of claims 16-17 and 22-23 in instant application is the combination with the inclusion of the following limitations:* **a module that, upon receiving a data write request as the data input/output request, writes data designated by the data write request in the disk drive device, and sends a write request for the data to the other disk array device.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Response to Applicant Remarks

The Applicant's Remarks has been carefully reviewed and is persuasive. Additional prior art references have been used in this Office Action to overcome the Applicant's arguments.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent Publication No. 2003/0159001 A1 to Chalmer et al. describes Distributed, scalable data storage facility with cache memory.

2. U. S. Patent No. 6,912,669 B2 to Hauck et al. describes Method and apparatus for maintaining cache coherency in a storage system.

3. U. S. Patent No. 6,321,298 B1 to Hubis describes Full cache coherency across multiple raid controllers.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information

for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

2006-03-29

DONALD SPARKS
SUPERVISORY PATENT EXAMINER